晶采光電科技股份有限公司
AMPIRE CO., LTD.

Specifications for LCD module

Customer	
Customer part no.	
Ampire part no.	AM-800480R3MZQW-A1H
Approved by	
Date	

☐ Preliminary Specification
■ Formal Specification

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Approved by	Checked by	Organized by
Patrick	Kokai	Jessica

This Specification is subject to change without notice.

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2021/12/27	--	New Release	Jessica

1. Introduction

It's a 7 inches Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. This module is composed of a 7" TFT-LCD panel, LED backlight.

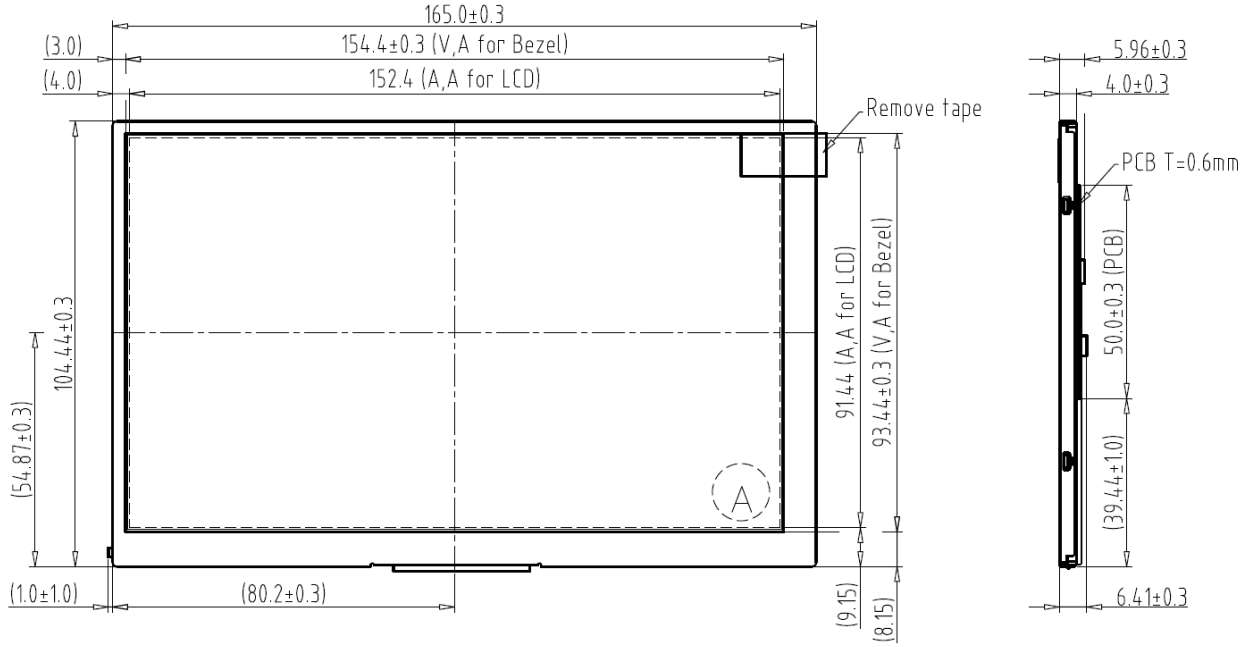
(1) Construction: 7" a-Si TFT active matrix, White LED Backlight.
(2) Resolution (pixel): 800(R.G.B) X480
(3) Number of the Colors: 262,144 colors (R, G, and B 6 bit digital each)
(4) LCD type: Transmissive, normally black
(5) Interface: LVDS

1.1 Features

(1) Input interface voltage : 3.3V

2. Physical Specifications

Item	Specifications	unit
LCD size	7 inch (Diagonal)	
Resolution	800 x (RGB) x 480	dot
Pixel pitch	0.1905 x 0.1905	mm
Color arrangement	RGB-stripe	
interface	Digital	



3. Absolute Max. Ratings

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power Voltage	VDD	-0.5	--	5	V	
Operation Temperature	TOP	-20	-	70	℃	
Storage Temperature	TST	-30	-	80	℃	

Note(1) The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

4. Electrical Characteristics

4.1 DC Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.2	3.3	3.4	V	
Input Voltage for logic	H Level	VIH	0.7 VDD	--	VDD	V	
	L Level	VIL	0	--	0.3 VDD	V	
(Panel+ LSI) Consumption Power		White Mode	--	**510**	**765**	mW	Note1

Note(1) TFT power supply current. VDD=3.0V, fV =60Hz, Ta=25℃, Display pattern: All White

LVDS DRIVER DC SPECIFICATIONS						
Differential Output Voltage	VOD	250	350	450	mV	RL=100ohm
Change in VOD between Complimentary Output States	ΔVOD	-	-	35	mV	
Common Mode Voltage	VOC	1.125	1.25	1.375	V	
Change in VOC between Complimentary Output States	ΔVOC	-	-	35	mV	
LVDS RECEIVER DC SPECIFICATIONS						
Differential Input High Threshold	VTH	-	-	+100	mV	VOC=+1.2V
Differential Input Low Threshold	VTL	-100	-	-	mV	

Note1: Ta=25℃, Display pattern: All Black

Note2: SDA, SCL, XRES.

4.2 AC Characteristics

LVDS

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{su}	Setup time, D0–D20 to CLKOUT↓	C_L = 8 pF, See Figure 5	5			ns
t_h	Data hold time, CLKOUT↓ to D0–D20		5			ns
$t_{(RSKM)}$	Receiver input skew margin§ (see Figure 7)	t_c = 15.38 ns (±0.2%), |Input clock jitter| < 50 ps¶,	550	700		ps
t_d	Delay time, CLKIN↑ to CLKOUT↓ (see Figure 7)	V_{CC} = 3.3 V, t_c = 15.38 ns (±0.2%), T_A = 25°C	3	5	7	ns
t_{en}	Enable time, $\overline{\text{SHTDN}}$ to phase lock	See Figure 7		1		ms
t_{dis}	Disable time, $\overline{\text{SHTDN}}$ to off state	See Figure 8		400		ns
t_t	Transition time, output (10% to 90% t_r or t_f) (data only)	C_L = 8 pF		3		ns
t_t	Transition time, output (10% to 90% t_r or t_f) (clock only)	C_L = 8 pF		1.5		ns
t_w	Pulse duration, output clock			0.50 t_c		ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
§ The parameter $t_{(RSKM)}$ is the timing margin available to allocate to the transmitter and interconnection skews and clock jitter. The value of this parameter at clock periods other than 15.38 ns can be calculated from t_{RSKM} = tc/14 – 550 ps.
¶ |Input clock jitter| is the magnitude of the change in input clock period.

PARAMETER MEASUREMENT INFORMATION

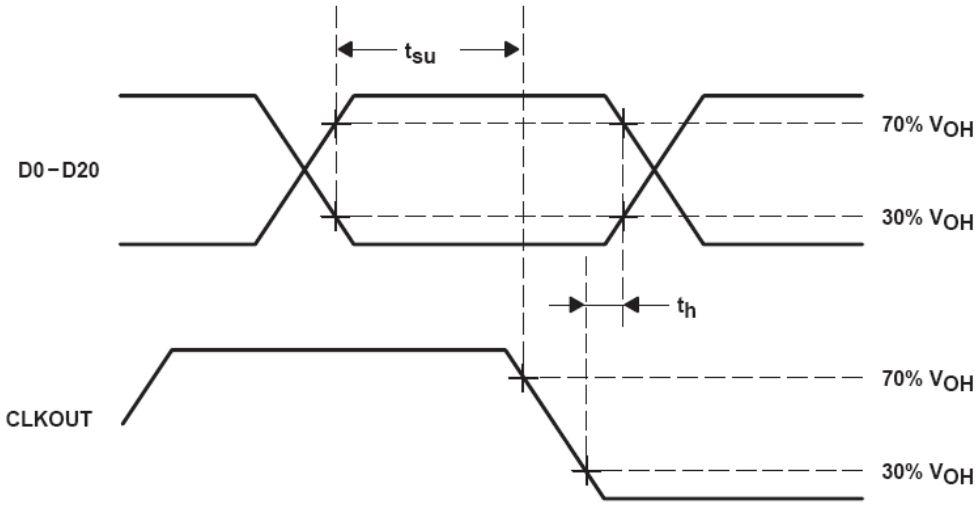


Figure 5. Setup and Hold Time Waveforms

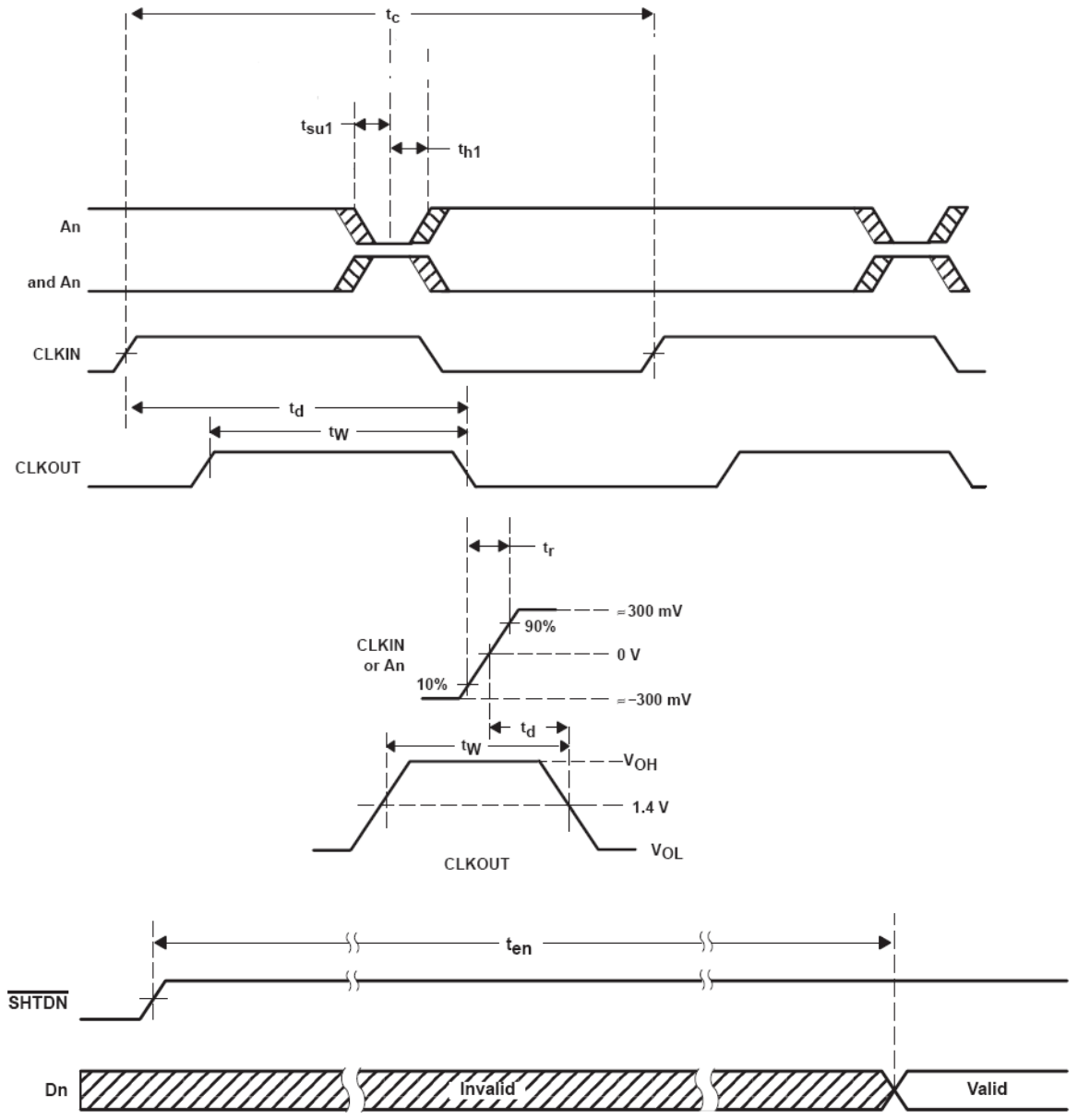


Figure 7. Enable Time Waveforms

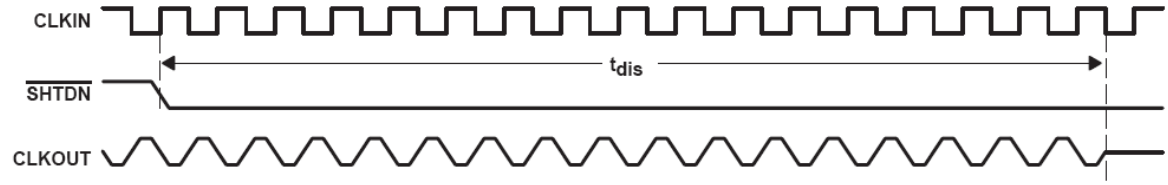


Figure 8. Disable Time Waveforms

TTL

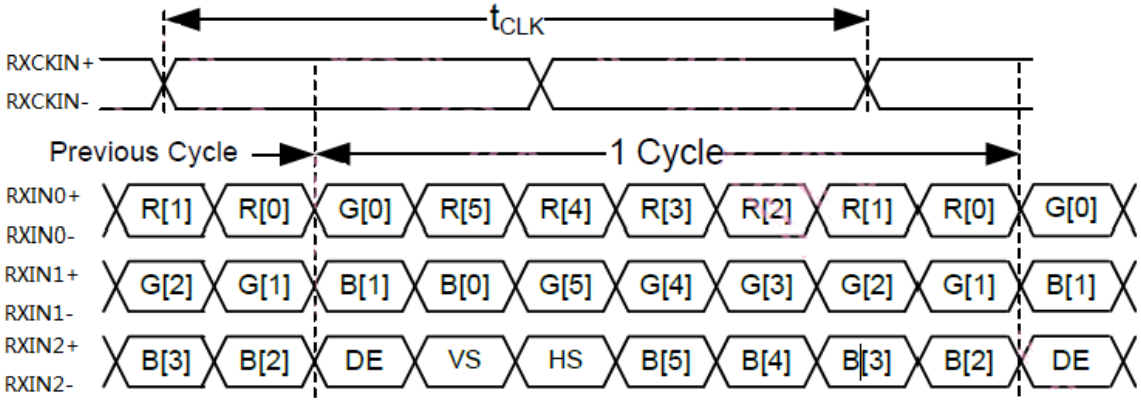
Horizontal Input Timing Table

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
DCLK frequency	fclk	20	33.3	42.8	MHz	
Horizontal display area	thd		800		DCLK	
1 Horizontal Line	th	908	928	1178	DCLK	
HSD pulse width	thpw	1	48	87	DCLK	thb+thpw=88 DCLK is fixed.
HSD Back Porch (Blanking)	thb	87	40	1	DCLK	
HSD Front Porch	thfp	20	40	290	DCLK	

Vertical Input Timing Table

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Vertical display area	tvd		480		H	
VSD period time	tv	517	525	606	H	
VSD pulse width	tvpw	1	1	3	H	Tvpw+tvb=32 H is fixed
VSD Back Porch (Blanking)	tvb	31	31	29	H	
VSD Front Porch	tvfp	5	13	94	H	

6-bit LVDS input interface



5. LED Driving Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
LED Driver Voltage	VLED	3.3	-	5	V	
Power Supply Current For LED Driver	ILED	-	TBD	-	mA	VLED=5V VADJ=3.3V (Duty 100%)
ADJ Input Voltage	V_{ADJ}	-	3.3	-	V	duty=100%
ADJ signal frequency	f_{PWM}	100	50K	200K	Hz	
ADJ signal logic level High	VIH	2V	--	VLED (5.0V)	V	
ADJ signal logic level Low	VIL	0	--	0.5	V	
LED Backlight Voltage	VAK	--	TBD	--	V	For reference IAK =TBDmA
LED Backlight Current	IAK	-	TBD	-	mA	Ta=25℃
LED Life Time			50K		Hr	Note(2)

Note(1) The backlight must be driven by constant current source.

Note(2) Brightness to be decreased to 50% of the initial value.

6. Interface

Pin No.	Symbol	Function
1	VDD	Power Supply:3.3V
2	VDD	Power Supply:3.3V
3	GND	Power Ground
4	GND	Power Ground
5	IN0-	Transmission Data of Pixels
6	IN0+	Transmission Data of Pixels
7	GND	Power Ground
8	IN1-	Transmission Data of Pixels 1
9	IN1+	Transmission Data of Pixels 1
10	GND	Power Ground
11	IN2-	Transmission Data of Pixels 2
12	IN2+	Transmission Data of Pixels 2
13	GND	Power Ground
14	CLK-	Sampling Clock
15	CLK+	Sampling Clock
16	GND	Power Ground
17	VLED	Power Supply for backlight : 5V
18	VLED	Power Supply for backlight : 5V
19	GND	Power Ground
20	ADJ	LED PWM SIGNAL

7. Optical Characteristics

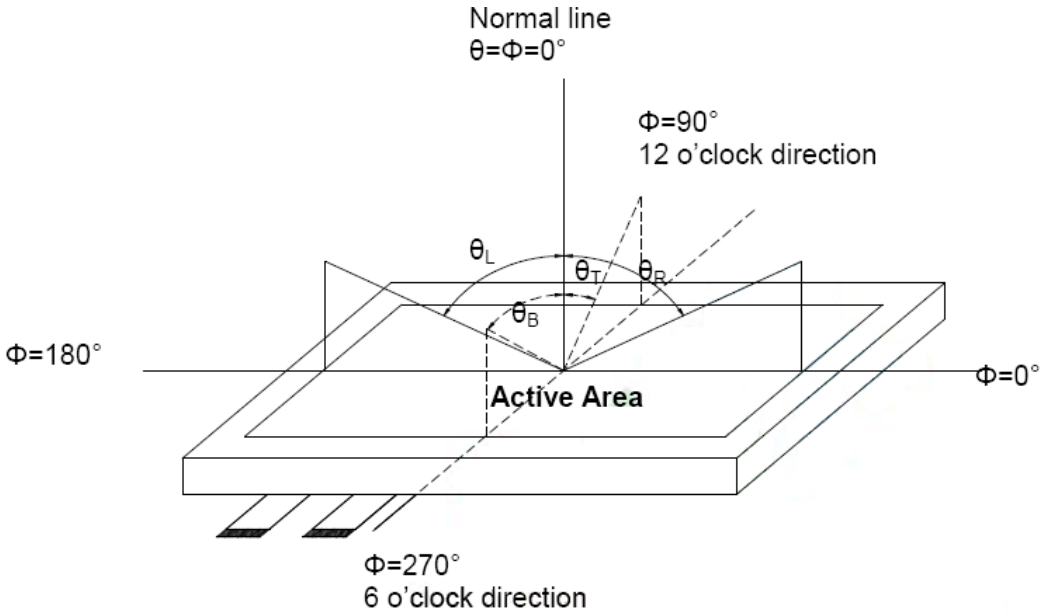
Item	Symbol	Condition	Values			Unit	Note
			Min.	Typ.	Max.		
Viewing angle (CR≧10)	θ L	Φ = 180° (9 o'clock)	80	85	--	degree	Note1
	θ R	Φ = 0° (3 o'clock)	80	85	--		
	θ T	Φ = 90° (12 o'clock)	80	85	--		
	θ B	Φ = 270° (6 o'clock)	80	85	--		
Response time	TON	25℃	--	20	30	msec	Note3
	TOFF					msec	
Contrast ratio	CR	Normal θ =Φ=0	800	1000	--	--	Note4
Color chromaticity	WX		Typ. -0.05	TBD	Typ. +0.05	--	Note5 Note6
	WY			TBD		--	
	RX			TBD			
	RY			TBD			
	GX			TBD			
	GY			TBD			
	BX			TBD			
	BY			TBD			
NTSC	--		65	70		%	Note5
Luminance (central point)	L		**400**	**500**	--	cd/m^2	Note6
Luminance uniformity	YU		70	75	--	%	Note6

Test Conditions:

VDD = 3.3V, IAK = TBDmA (Backlight current), the ambient temperature is 25℃.

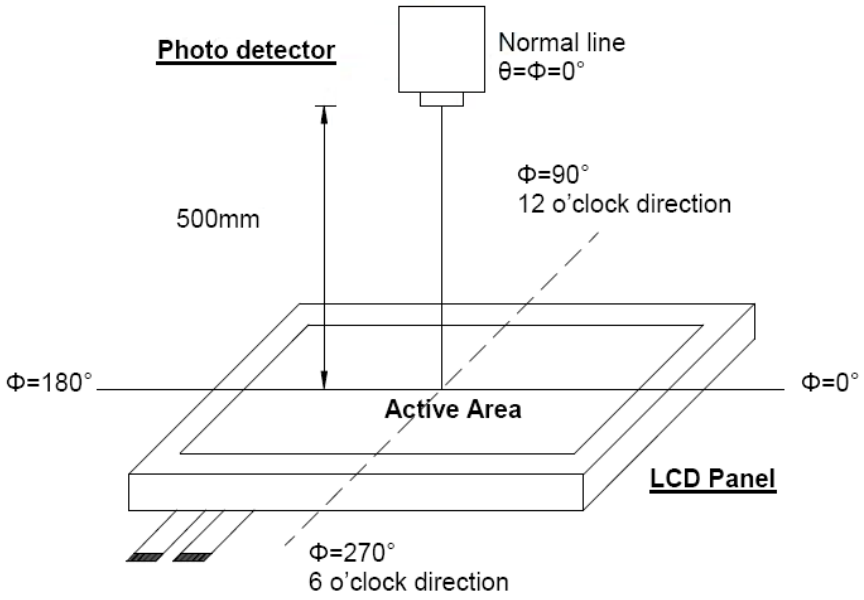
The test systems refer to Note 2.

Note(1) Definition of viewing angle range



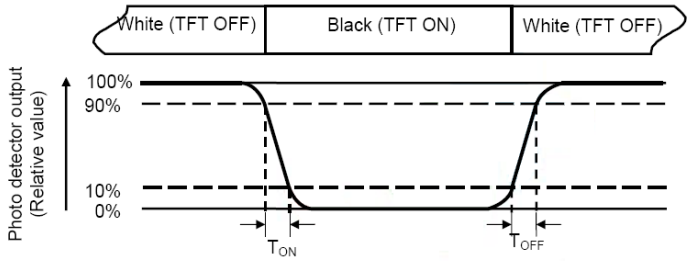
Note(2) Definition of optical measurement system

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view: 1° / Height: 500mm.)



Note(3) Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note(4) Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note(5) Definition of color chromaticity (CIE1931)

Color coordinated measured at center point of LCD.

All input terminals LCD panel must be ground when measuring the center area of the panel.

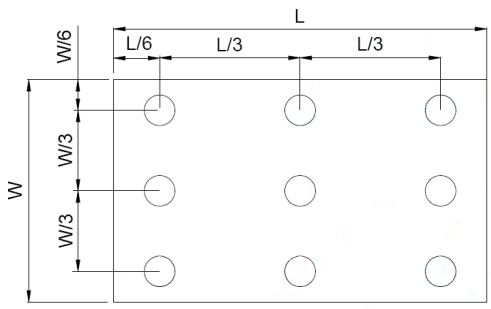
Note(6) Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to bellow figure).

Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity (Yu)} = \frac{Bmin}{Bmax}$$

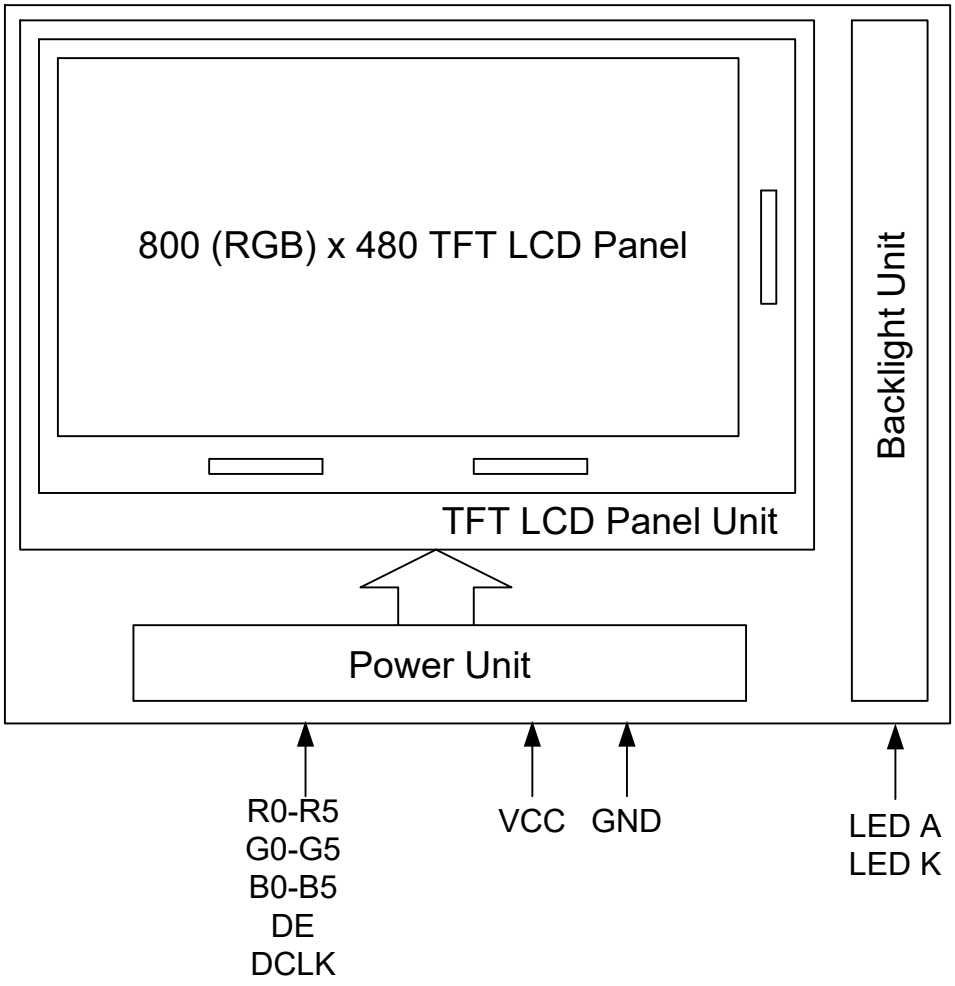
L ----- Active area length W ----- Active area width



Bmax : The measured maximum luminance of all measurement position.

Bmin : The measured minimum luminance of all measurement position.

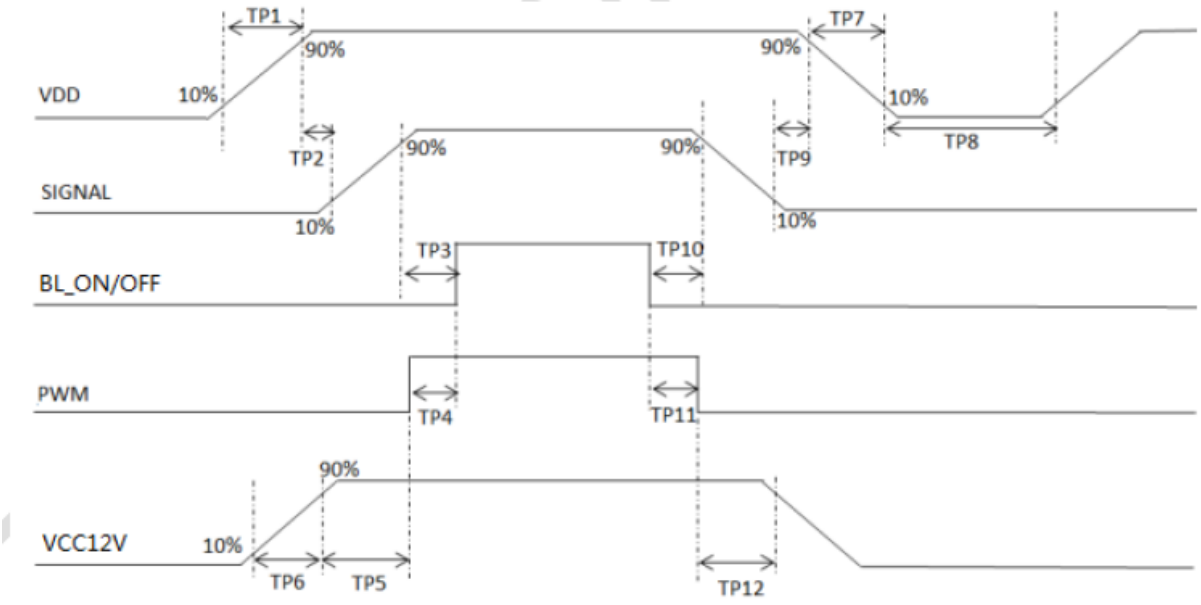
8. Block Diagram



9. Power ON/OFF sequence

Item	Symbol	MIN	Typ	MAX	Unit	Remark
VDD on to VDD stable	Tp1	0.5	-	10	ms	
VDD stable to signal on	Tp2	0	-	50	ms	
Signal stable to BL_ON/OFF on	Tp3	200	-	-	ms	
PWM on to BL_ON/OFF on	Tp4	0	-	200	ms	
VCC12V to PWM on	Tp5	10	-	-	ms	
VCC12V on to VCC12V stable	Tp6	0.5	-	10	ms	
VDD off time	Tp7	0.5	-	10	ms	
VDD off to next VDD on	Tp8	500	-	-	ms	
Signal off before VDD off	Tp9	0	-	500	ms	
BL_ON/OFF off before signal off	Tp10	200	-	-	ms	
BL_ON/OFF off before PWM off	Tp11	0	-	200	ms	
PWM off before VCC12V off	Tp12	10	-	-	ms	

Table 5.2 Power on/off sequence



10. Reliability Test Conditions

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C ,Dry t=240 hrs	
Low Temperature Operation	-20±3°C, Dry t=240 hrs	
High Temperature Storage	80±3°C , Dry t=240 hrs	1,2
Low Temperature Storage	-30±3°C ,Dry t=240 hrs	1,2
Humidity Test	60 °C, Humidity 90%, 240 hrs	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note(1) Condensation of water is not permitted on the module.

Note(2) The module should be inspired after 1 hour storage in normal conditions (15~35℃, 45~65%RH).

Note(3) The module shouldn't be tested over one condition, and all the tests are independent.

Note(4) All reliability tests should be done without the protective film.

Definitions of life end point:

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of initial value.

11. Use Precautions

11.1 Handling precautions

(1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.

(2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.

(3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.

(4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

11.2 Installing precautions

(1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.

(2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.

(3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.

(4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off

11.3 Storage precautions

(1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.

(2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.

(3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

11.4 Operating precautions

(1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.

(2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.

(3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.

(4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.

(5) Make certain that each signal noise level is within the standard (L level: 0.2VDD or less and H level: 0.8VDD or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.

(6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.

(7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

(8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

11.5 Other

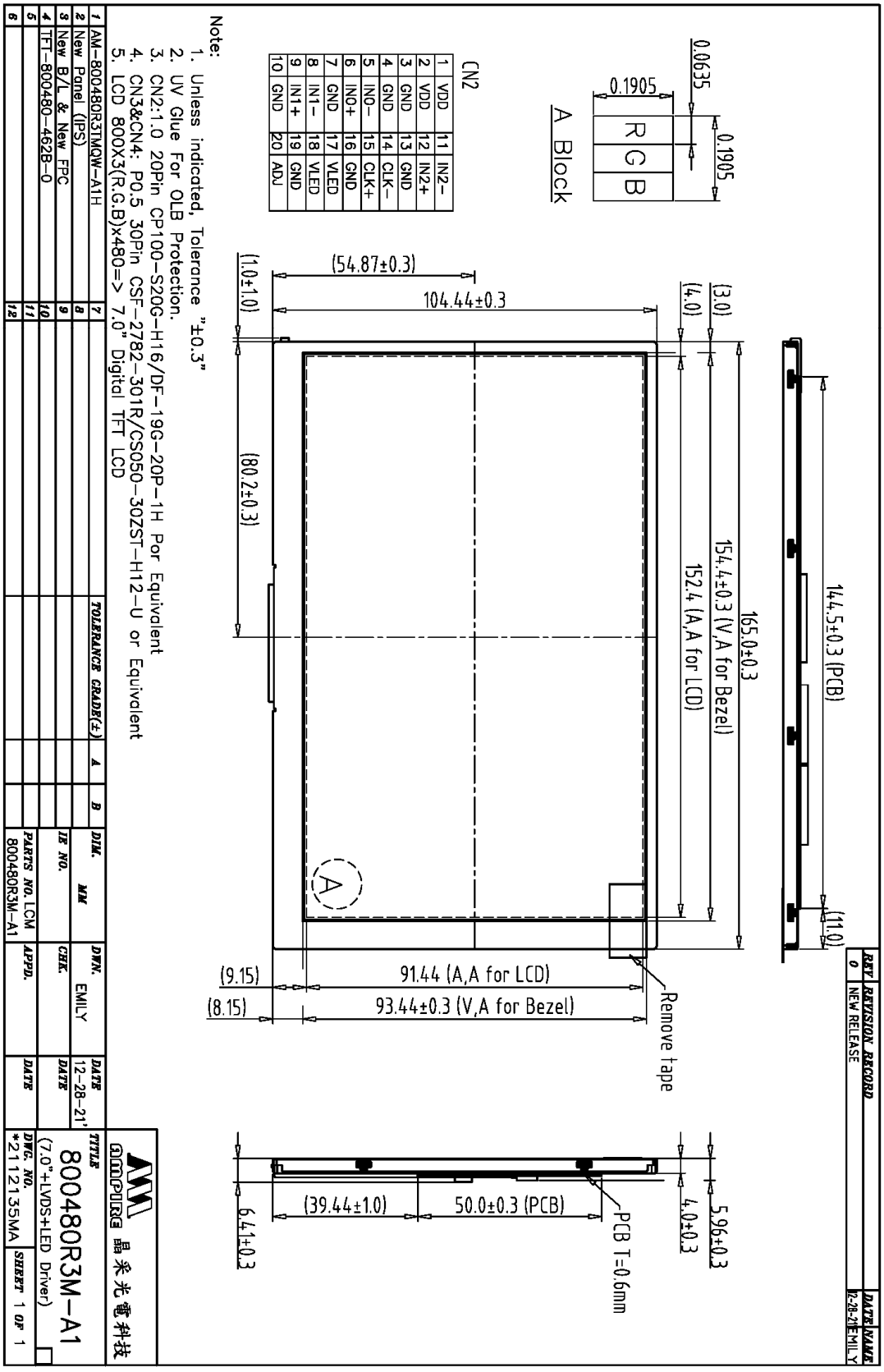
(1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.

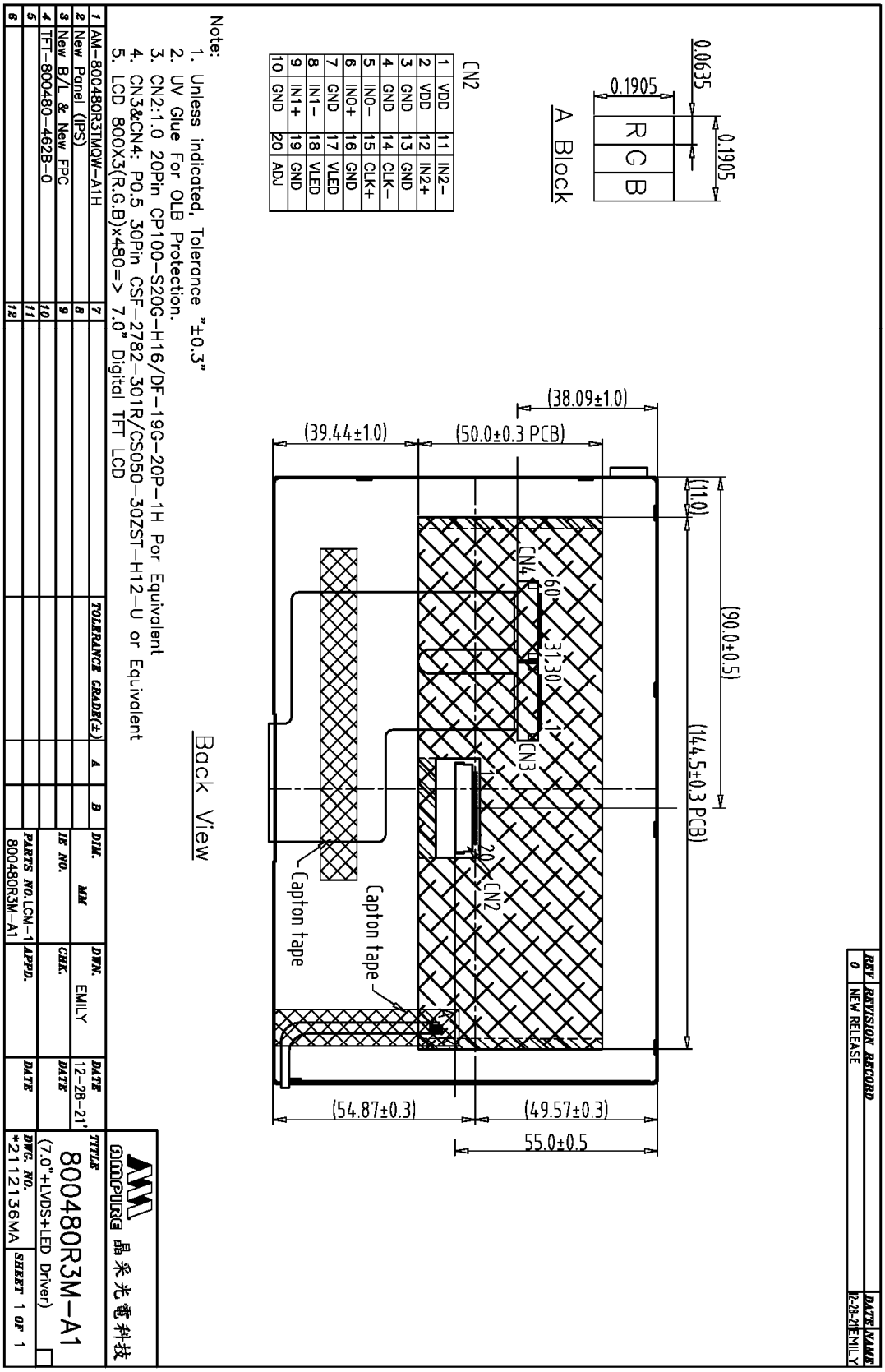
(2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.

(3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

(4) Do not keep the LCD at the same display pattern continually. The residual image will happen and it will damage the LCD. Please use screen saver.

12. Outline Dimension




REV. REVISION RECORD
DATE NAME
0 NEW RELEASE
12-28-21 EMILY
A Block
0.1905
0.0635
0.1905
R G B
CN2
1 VDD 11 IN2-
2 VDD 12 IN2+
3 GND 13 GND
4 GND 14 CLK-
5 IN0- 15 CLK+
6 IN0+ 16 GND
7 GND 17 VLED
8 IN1- 18 VLED
9 IN1+ 19 GND
10 GND 20 ADJ
Back View
(38.09±1.0)
(39.44±1.0)
(50.0±0.3 PCB)
(11.0)
(90.0±0.5)
(144.5±0.3 PCB)
CN4
60°
31.30
CN3
20
CN2
Capton tape
Capton tape
(54.87±0.3)
(49.57±0.3)
55.0±0.5
Note:
1. Unless indicated, Tolerance "±0.3"
2. UV Glue For OLB Protection.
3. CN2:1.0 20Pin CP100-S20G-H16/DF-19G-20P-1H Por Equivalent
4. CN3&CN4: P0.5 30Pin CSF-2782-301R/CS050-30ZST-H12-U or Equivalent
5. LCD 800X3(R.G.B)x480=> 7.0" Digital TFT LCD
1 AM-800480R3TMQW-A1H
2 New Panel (IPS)
3 New B/L & New FPC
4 TFT-800480-462B-0
TOLERANCE GRADE(±) A B DIM. MM
DWN. EMILY
CHK.
APPD.
DATE 12-28-21'
DATE
DATE
PARTS NO. LCM-1 800480R3M-A1
JIS NO.
AMPIRE 晶采光電科技
TITLE 800480R3M-A1
(7.0"+LVDS+LED Driver)
DWG. NO. *2112136MA
SHEET 1 OF 1

13. Package

TBD